AMENDMENTS TO THE SPECIFICATION AND ABSTRACT

Please amend the paragraph [0019] beginning on page 8, as follows:

[0019] [FIG. 1] FIG. 1 is a functional block diagram showing a configuration of a three-dimensional shape drawing device according to an embodiment of the present invention.

~~[FIG. 2] FIG. 2 is a diagram schematically showing a depth value retained by a high order Z-buffer memory 102 and a low order Z-buffer memory 104.~~

[FIG. ~~3~~ 2] FIG. ~~3~~ 2 is a flowchart showing operations of the three-dimensional shape drawing device shown in FIG. 1.

[FIG. ~~4~~ 3] FIG. ~~4~~ 3 is a flowchart showing a detailed process at subroutine step S19 shown in FIG. 3.

[FIG. 4] FIG. 4 is a diagram schematically showing a depth value retained by a high order Z-buffer memory 102 and a low order Z-buffer memory 104.

[FIG. 5] FIG. 5 is a block diagram showing an exemplary hardware configuration of the three-dimensional shape drawing device.

[FIG. 6] FIG. 6 is a block diagram showing an exemplary hardware configuration of the three-dimensional shape drawing device.

[FIG. 7] FIG. 7 is a block diagram showing a configuration of a three-dimensional shape drawing device 200 described in a patent document 2.

[FIG. 8] FIG. 8 schematically shows a screen 214 for displaying a three-dimensional shape drawn by the three-dimensional shape drawing device of FIG. 7 and a configuration of a ZR buffer 205.

Please amend the paragraph [0024] beginning on page 12, as follows:

[0024] Controlled by a timing control section 109 is a timing of drawing a figure to show a next display when a previous display is completed. To be specific, at a timing when the figure should be drawn for the next display, the timing control section 109 instructs the high order Z-buffer clearing section 107 and the low order clearing section 108 ~~Z-buffer memory 104~~ to initialize the image memory 103, the high order Z-buffer memory 102 and the low order Z-buffer memory 104. Also, the timing control section 109 instructs

the drawing section 101 to start drawing the figure at the timing when the figure should be drawn for the next display.

Please amend the paragraph [0026] beginning on page 12, as follows:

[0026] The high order bit comparing section 105 compares high order bits of a depth value received from a later-described depth value calculation section 110 with high order bits of a depth value read from the high order Z-buffer memory 102. The high ~~low~~ order bits which the high order bit comparing section 105 reads from the high order Z-buffer memory 102 are high ~~low~~ order bits of a depth value of a pixel which is in a same position as that of a pixel which the depth value calculation section 110 has used for calculation. Then, the high order bit comparing section 105 notifies a comparison result of the two sets of high order bits to a later-described read control section 112.

Please amend the paragraph [0035] beginning on page 17, as follows:

[0035] FIGS. 2 and 3 are flow charts showing operations of the three-dimensional shape drawing device 10 shown in FIG. 1. First, when a displaying process of a previous display is completed, the timing control section 109 instructs the high order Z-buffer clearing section 107 to initialize the image memory 103 and the high order Z-buffer memory 102. Then, the high order Z-buffer clearing section 107 initializes the high order Z-buffer memory 102 and the image memory 103, and overwrites, with an initial value, values retained by the high order Z-buffer memory 102 and the image memory (Step S11). The initial value is, for example, a depth value indicating a farthest point from a viewpoint. Hereinafter, an example will be described in which a depth value is represented in hexadecimal, and the depth value indicating the farthest point is 000000H in 24 bits. For example, when high order bits are 8 bits, the high order Z-buffer clearing section 107 initializes the high order Z-buffer memory 102 by using 00H at step S11.

Please amend the paragraph [0048] beginning on page 21, as follows:

[0048] In an example shown in FIG. 4, since the high order Z-buffer memory 102 retains high order 8 bits, and the low order Z-buffer memory 104 retains low order 16 bits, the high order Z-buffer clearing section 107 initializes a value retained by the high order Z-

buffer memory 102 to 00H, and the low order Z-buffer clearing section 108 initializes a value retained by the low order Z-buffer memory 104 to 0000H. Note that, instead of having the high order Z-buffer clearing section 107 and the low order Z-buffer clearing section 108 which are dedicated to initializing the high order Z-buffer memory 102 and the low order Z-buffer ~~clearing section 108~~ memory 104, the drawing section 101 may have a function for overwriting the values retained by the high order Z-buffer memory 102 and low order Z-buffer memory 104 with the value 000000H indicating the farthest point.

Please amend the paragraph [0063] beginning on page 28, as follows:

[0063] High-speed processing is realized by using the high-speed graphics memory being capable of high-speed processing as the high order Z-buffer memory which is accessed more frequently than the low order Z-buffer memory and image memory. Since the high ~~low~~ order Z-buffer memory is only required to retain high order 8 bits of a depth value, a necessary size of the high-speed graphics memory can be kept small. Moreover, a processing speed of the three-dimensional shape drawing device can be enhanced with a minimum increase in cost, by including, in the low-speed graphics memory which has a large capacity but is low-speed, the low order Z-buffer memory and the image memory which are accessed less frequently than the high order Z-buffer memory.

Please amend the paragraph [0067] beginning on page 29, as follows:

[0067] FIG. 6 is a block diagram showing a hardware configuration of the three-dimensional shape drawing device 10 in the case where the image memory 103 and the low order Z-buffer memory 104 are external memories. In FIG. 6, the three-dimensional shape drawing device comprises the CPU 121, an embedded memory 124 and a memory I/F 125, the CPU 121 implementing the function of the drawing section 101.